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TIMOTHY N TROP  
TROP PRUNER HU & MILES PC  
8554 KATY FREEWAY STE 100  
HOUSTON, TX 77024

EXAMINER

MEONSKE, TONIA L

ART UNIT

PAPER NUMBER

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Paper No. 11

Application Number: 09/465,634  
Filing Date: December 17, 1999  
Appellant(s): VAVRO ET AL.

\_\_\_\_\_  
Timothy N. Trop  
For Appellant

**MAILED**

**FEB 10 2003**

**Technology Center 2100**

**EXAMINER'S ANSWER**

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This is in response to the appeal brief filed January 15, 2003.

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

No amendment after final has been filed.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) *Grouping of Claims***

Examiner acknowledges that Applicant has grouped claims 1-15 separately from claims 16-24, whereby claims 1-15 rise and fall with claim 1 and claims 16-24 rise and fall with claim 16. However, the Board is advised that the Applicant has failed to include reasons to support the grouping. Applicant has not explained how the two groups of claims differ in scope and are patentably distinct from each other. See 37 CFR 1.192(c)(7). The only difference that Examiner notes is that claims 1-15 are device claims and claims 16-24 are method claims.

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Furthermore, it is noted that the element of dispute is the term “mathematical”, which refers to a claimed processor, appears in both the method and device claim groups, in claim 1 and claim 16. Since the element of dispute appears in both groups of claims, Examiner Suggests that the Board group claims 1-24 together, whereby claims 1-24 rise and fall with claim 1.

**(8) *Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) *Prior Art of Record***

EP 0 942 603

Kitamura et al.

9-1999

**(10) *Grounds of Rejection***

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 112***

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The claim recites the limitation “wherein said mathematical processor is a multi-cycled mathematical processor.” This language is unclear because since the word “cycle” is a measurement of time, it is unclear how a processor can be multi-timed. This phraseology in the claims may have the following two accepted meanings: 1) the processor requires multiple cycles to complete an operation, or 2) the processor is operated at various cycle speeds. In order to clear up this interpretation discrepancy, Examiner tried to identify which portion of the specification in which Applicant refers in order to interpret the term “multi-cycled”. However, there is support for both interpretations in the specification. On page 24, lines 20-23, Applicant discloses a multi-cycle operation on a processor which may take more than one cycle to

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complete, which supports the first meaning of the phraseology. On page 23, line 19, Applicant discloses a multi-cycle mathematical processor that is operated at various speeds, which supports the second meaning. After reading claim 15 in light of the specification, claim 15 is still indefinite. For the purposes of examination, the first meaning is assumed.

***Claim Rejections - 35 USC § 102***

Claims 1-4, 6, 8, 9, 15, 16, 17, 23, and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura). Referring to claim 1, Kitamura has taught a digital signal processor comprising:

- a. a mathematical processor (Kitamura column 9, line 58 to column 10, line 1 and figure 6, element 5, column 26, lines 39-50);
- b. an input processor that processes input signals to the digital signal processor (Kitamura column 10, line 28 to column 11, line 8 and figure 6, element 3);
- c. an output processor that processes output signals from the digital signal processor (Kitamura column 12, lines 15-52 and figure 6, element 6);
- d. a master processor that controls said mathematical processor, said input processor and said output processor (Kitamura column 10, lines 1-2 and figure 6, element 7); and
- e. a storage selectively accessible by each of said processors (Kitamura column 10, lines 21-27 and figure 6, element 10).

Referring to claim 2, Kitamura has taught the digital signal processor further including a random access memory processor that stores intermediate calculation results (Kitamura column 12, lines 10-14).

Referring to claim 3, Kitamura has taught the digital signal processor including a bus coupling each of said processors to said storage (Kitamura figure 6, element 9).

Referring to claim 4, Kitamura has taught the digital signal processor wherein said input and output processors also implement mathematical operations (Kitamura column 10, line 28 to column 11, line 8, column 12, lines 15-52 and figure 6, elements 3 and 6).

Referring to claim 6, Kitamura has taught the digital signal processor wherein said processors communicate with one another through said storage (Kitamura column 10, lines 15-17 and 28-32, column 11, lines 47-55, and column 12, lines 15-20).

Referring to claim 8, Kitamura has taught the digital signal processor wherein said master processor provides the timing for the other processors (Kitamura column 10, lines 5-14 where the master processor determines the timing for when the processors execute instructions because it controls when the instructions are sent).

Referring to claim 9, Kitamura has taught the digital signal processor wherein said master processor waits for the input processor to complete a given operation (Kitamura column 6, lines 3-20 and column 11, lines 47-49 where the signal must be processed in the input processor before being spliced by the data processing unit as per the control of the master processor, therefore, the master processor must wait for the input processor to complete its operation).

Referring to claim 15, Kitamura has taught the digital signal processor wherein said mathematical processor is a multi-cycled mathematical processor (Kitamura column 11, lines 46-55 where an operation takes multiple cycles to complete).

Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

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Claim 17 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

***Claim Rejections - 35 USC § 103***

Claims 5, 7, 14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura). Referring to claim 5, Kitamura has not explicitly taught each of said processors having their own instruction sets. However, Kitamura has taught a mathematical processor, an input processor, an output processor, and a master processor each with divergent functionality. Since the definition of an instruction set is that combination of commands which allows a processor to appropriately perform its defined functions, it would be readily acknowledged by an artisan that the plural processors as taught by Kitamura must each have their own instruction set. That is, the instructions required to perform the input processing, mathematical functions, control, and output processing must be different from one another. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recreate the plural processors of Kitamura where each has its own instruction set. Official notice has been taken.

Referring to claim 7, Kitamura has not explicitly taught each processor using very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for the processors of Kitamura to be issued several instructions at once and ensured, by the nature of VLIW instructions, that the compiler would have only combined instructions that are not dependent upon one another. Therefore, it would have been obvious to a

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person of ordinary skill in the art at the time the invention was made to employ the very long instruction word format for instructions issued to the plural processors of Kitamura in order to increase speed and efficiency of those processors. Official notice has been taken.

Referring to claim 14, Kitamura has not explicitly taught a mathematical pipeline which is pipelined. However, Kitamura has taught a mathematical processor that requires multiple cycles to complete a given operation, i.e. at least one cycle for memory access and one cycle for execution (Kitamura column 11, lines 51-55). The concept of pipelining is well known in the art and would have been beneficially employed in the mathematical processor of Kitamura in order to increase efficiency by overlapping the steps of memory access and execution for each processed instruction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the well known concept of pipelining to the mathematical processor in order to increase efficiency and speedup. Official notice has been taken.

Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of Whittaker et al., U.S. Patent Number 5,968,167 (hereinafter Whittaker). Kitamura has not explicitly taught the digital signal processor wherein each of said processors includes its own random access memory. Whittaker has taught each of a plurality of processors including its own random access memory (Whittaker column 6, lines 56-65). The RAMs of Whittaker provide storage for those instructions to be executed by each processor. As discussed above in the



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rejection of claim 5, each processor of Kitamura has its own instruction set and those instructions are issued to each processor by the master processor. Therefore, it would have been beneficial to employ separate RAMs for each processor such that the master processor would have required less logic to inform each processor to access its RAM and fetch its own next instruction, rather than the master accessing the main storage, determining which processor the instruction belonged to, and then physically issuing that instruction to the slave processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ individual RAMs for each of the plural processors of Kitamura, as taught by Whittaker in order to allow for a simpler master processor.

Claims 11-13, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of Nakagawa et al., U.S. Patent Number 5,241,679 (hereinafter Nakagawa). Referring to claim 11, Kitamura has not taught the digital signal processor wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register. Nakagawa has taught a storage including a plurality of registers (Nakagawa figure 1), where the registers automatically transfer existing data from a first register to a second register when new data is written into the first register (Nakagawa column 4, line 53 to column 5, line 16 and figure 2). Replacing the storage of Kitamura with the multi-register storage of Nakagawa would have allowed for the contents of all the registers to be saved, in case of an interrupt or context switch, simultaneously to the dedicated stack memories in order to perform both saving and restoration at a high speed (Nakagawa column 2, lines 17-23 and 42-49). Therefore, it would have been obvious to a person

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of ordinary skill in the art at the time the invention was made to employ the multi-register storage system of Nakagawa instead of the generic storage means in the system of Kitamura in order to increase the speed at which context preserving and restoration occurs.

Referring to claim 12, Nakagawa has taught the digital signal processor wherein said input processor causes the automatic transfer of data (Nakagawa column 4, line 53 to column 5, line 16 where the processor causing the data to be stored is necessarily an input processor).

Referring to claim 13, Nakagawa has taught the digital signal processor wherein the mathematical processor causes said data to be transferred from one register to another (Nakagawa column 4, line 53 to column 5, line 16).

Claim 18 does not recite limitations above the claimed invention set forth in claim 11 and is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

Claim 19 does not recite limitations above the claimed invention set forth in claim 12 and is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

Claim 20 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

Referring to claim 21, Nakagawa has taught storing a bit which indicates which processor may controls aid automatic transfer of data from one register to another (Nakagawa column 2, lines 29-33).

**(11) Response to Argument**

***Response to Argument-Claim Rejections - 35 USC § 112***

- On pages 15-16 of the Appeal Brief, Applicant argues in essence:

*"Claim 15 was rejected on the grounds that the word "multi-cycled" is indefinite. With respect to the objection to the term "multi-cycled" mathematical processor, a multi-cycle element is explained on page 24, line 15 through page 25, line 16 (and as explained in the material set forth in the summary herein at page 14, last paragraph through the end.*

*As explained on page 14 infra, the use of multi-cycled elements allows interchangeability without affecting the instruction decode. A busy signal can be used to hold off new data from being sourced to the ineffectuated unit. Internal delays may be used to match latency such that multi-cycle operation occurs. This allows the various processors in the overall system to be exchanged and changed out regardless of whether they may involve operations spread over two or more clock cycles. For example, input data valid and input destination signals may be delayed that needed number of cycles to make different processors working on different cycles coherent.*

*Different multi-cycled mathematical processors may be added to the overall process regardless of whether they require more or less time than the processor which they replace. Thus, in cases where a slower math processor is replacing a faster math processor, a multi-cycled architecture may be used to compensate for the additional delay time. The MPC 18 is recompiled when a new processor that is slower or faster is added to adjust to the slower or faster timer of the new processor."*

Applicant has claimed a “multi-cycled mathematical processor”, not a “multi-cycled master processor”. However, Applicant is appearing to argue that the master processor is multi-cycled... not the mathematical processor. On page 25, lines 9-24 of Applicant’s specification, Applicant describes a multi-cycled architecture which is controlled by the master programmable controller. The master programmable controller adjusts to the speed of the processor, in order to support a processor no matter what its speed. This appears to be what Applicant is arguing.

It is clear from Applicant’s own admissions above that a certain processor has a certain speed, where certain processors are faster than other certain processors. For one of ordinary skill in the art, “multi-cycled mathematical processor” is interpreted at least two ways: 1) the processor requires multiple cycles to complete an operation and 2) that it is operated at various cycle speeds. The way Applicant is arguing to interpret “Multi-cycled mathematical processor” is much different than the way one of ordinary skill in the art would interpret “Multi-cycled mathematical processor”. It is not clear from reading the claims as to exactly what a Multi-cycled mathematical processor is. Furthermore the specification does not specifically clarify what a Multi-cycled mathematical processor is. There is support for both interpretations in the specification. On page 24, lines 20-23, Applicant discloses a multi-cycle operation on a processor which may take more than one cycle to complete, which supports the first meaning of this phraseology. On page 23 line 19, Applicant discloses a mutli-cycle mathematical processor that is operated at various speeds, which supports the second meaning. After reading claim 15 in light of the specification, it is still unclear as to what the metes and bounds are of the claim. Therefore claim 15 is indefinite.

***Response to Argument-Claim Rejections - 35 USC § 102***

- On pages 16-17 Applicant argues with respect to claim 1 in essence:

*“However, as indicated in column 11 of Kitamura, paragraph 39, beginning at line 47, the data processing unit 5 splices the video data DA and DB in response to a splicing instruction from CPU 7. There is no indication that this device can be considered to be a mathematical processor. Thus, at least one element is missing in Kitamura and, therefore the Sections 102 rejection should be reversed.*

*With respect to the argument that, in essence, “mathematical processor” simply means any processor, it is clear this cannot be so since mathematical processor is a well known term of art. Clearly mathematical processors are processors devoted to doing mathematical operations such as add and subtract. See, e.g., page 5, lines 17-24. This understanding is further supported by the attached academic paper.*

*Therefore, the rejection of claim 1, should be reversed.”*

However, “Mathematics” as defined by Merriam-Webster’s Collegiate Dictionary, Tenth Edition (see attached) is:

*“ the science of numbers and their operations, interrelations, combinations, generalizations, and abstractions and of space configurations and their structure, measurement, transformations, and generalizations.”*

Kitamura has taught that data processing unit 5 splices the video data DA and DB in response to a splicing instruction. DA and DB are encoded video data, which are combinations of bits, or numbers. (Kitamura, Column 11, lines 20-25) Since the data

processing unit 5, operates on, or splices numbers representing the coded video data DA and DB, the data processing unit, as taught by Kitamura, is a mathematical processor. Furthermore, more specifically, Kitamura has taught in column 26 that the blanking generator 20 (which is included as a part of the mathematical processor, element 5, See Figure 6) “produces blanking data  $D_{BLK}$  by setting a differential value between a macroblock and a reference macroblock...” (column 26 lines 45-50). A differential as defined by Microsoft Press Computer Dictionary, Second Edition (see attached) is:

*“In electronics, a reference to a type of circuit that makes use of the difference between two signals rather than the difference between one signal and some reference voltage.”*

Accordingly, in order to set a differential value or number, the difference of two numbers must be calculated. “Difference” as defined by Microsoft Press Computer Dictionary, Second Edition (see attached) is:

*“The amount by which two values differ. In arithmetic, the difference is the result of subtracting one number from another. In electronics, differences in physical elements, such as waveforms or voltages, are used in the operation of circuits, amplifiers, multiplexers, communications equipment, and so on.... ”*

Therefore, in order to calculate the difference between two numbers, a subtraction of the two numbers must be performed. Subtraction is clearly a mathematical operation, as admitted by Applicant in the argument above. The processor of Kitamura, element 5, is a mathematical processor because when it sets the differential value between a macroblock and a reference macroblock, it is performing a mathematical operation.

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- On page 17 Applicant argues with respect to claim 16 in essence:

*“Similarly, claim 16 calls for using a third processor for mathematical operations. No such thing is shown in Kitamura.”*

However, as proven above, Kitamura has in fact taught a third processor for mathematical operations. (Figure 6, element 5) Therefore, Kitamura has in fact taught each and every limitation in 16.

For the above reasons, it is believed that the rejections should be sustained.

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Respectfully submitted,

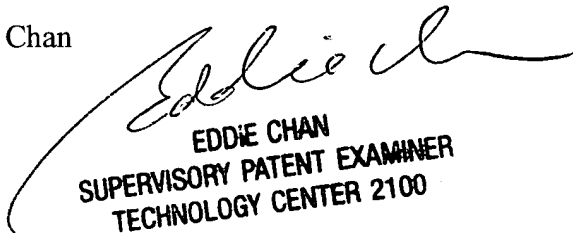
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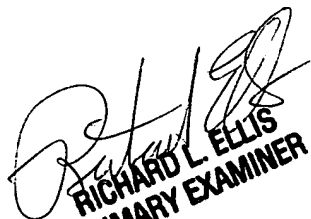
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Conferees:

Eddie Chan

  
EDDIE CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100

Richard Ellis  


  
RICHARD L. ELLIS  
PRIMARY EXAMINER

TIMOTHY N TROP  
TROP PRUNER HU & MILES PC  
8554 KATY FREEWAY STE 100  
HOUSTON, TX 77024



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## CONTRIBUTORS

JoAnne Woodcock  
*Senior Contributor*

Peter Aitken	Charles Petzold
Andrew Himes	Phil Rose
Chris Kinata	David Rygmyr
William G. Madison	Michael Vose
Ross Nelson	Bruce Webster
Wallace Parker	

## TECHNICAL REVIEWERS

Robert Ackerman	James Johnson
Steve Bostwick	Chris Kinata
Keith Burgoyne	Cary Lu
Kaare Christian	M. David Stone
Ray Duncan	John Viescas

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**dibit** Pronounced "dye-bit." A set of two bits representing one of four possible combinations: 00, 01, 10, and 11. In communications, a dibit is a kind of transmission unit made possible by the modulation technique known as differential phase-shift keying, which encodes data by using four different states (phase shifts) in the transmission line to represent each of the four dibit combinations. *See also* phase-shift keying.

**dichotomizing search** *See* binary search.

**DIF** *See* data interchange format.

**difference** The amount by which two values differ. In arithmetic, the difference is the result of subtracting one number from another. In electronics, differences in physical elements, such as waveforms or voltages, are used in the operation of circuits, amplifiers, multiplexers, communications equipment, and so on.

In database management, an operator in the relational algebra used in sorting records (tuples). For example, given two relations (tables), A and B, that are union-compatible (contain the same number of fields, with corresponding fields containing the same types of values),

#### DIFFERENCE A, B

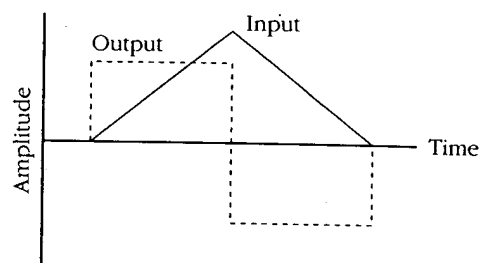
builds a third relation containing all those records that appear in A but not in B. *Compare* intersect, union.

**Difference Engine** An early computerlike mechanical device designed by British mathematician and scientist Charles Babbage in the early 1820s. Although never completed by Babbage, the Difference Engine was intended to be a machine with a 20-decimal capacity capable of solving mathematical problems. The concept of the Difference Engine was enhanced by Babbage in the 1830s in the design of his more famous Analytical Engine, a mechanical precursor of the electronic computer. Babbage, incidentally, was also the inventor of the speedometer and the cowcatcher. *See also* Analytical Engine.

**differential** In electronics, a reference to a type of circuit that makes use of the difference between two signals rather than the difference between one signal and some reference voltage.

**differential phase-shift keying** *See* phase-shift keying.

**differentiator** A circuit whose output is the differential (first derivative) of the input signal. The differential measures how fast a value is changing, so the output of a differentiator is proportional to the instantaneous rate of change of the input signal, as shown in the illustration. *Compare* integrator.



#### Differentiator.

*An example of the action of a differentiator circuit.*

**digit** One of the characters used to indicate a whole number (unit) in a numbering system. In any numbering system, the number of possible digits is equal to the base, or radix, used. For example, the decimal (base-10) system has 10 digits, 0 through 9; the binary (base-2) system has two digits, 0 and 1; and the hexadecimal (base-16) system has 16 digits, 0 through 9 and A through F.

**digital** Related to digits or the way they are represented. In computing, *digital* is virtually synonymous with *binary* because the computers familiar to most people process information coded as combinations of binary digits (bits). One bit can represent at most two values; 2 bits, four values; 8 bits, two hundred fifty-six values; and so on. Values that fall between two numbers are represented as either the lower or the higher of the two. Because digital representation represents a value as a coded number, the range of values represented can be very wide, although the number of possible values is limited by the num-

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